

REMARKS

Claims 1 to 12 and 14 to 15 remain in the present application. Claims 1, 3, 4, 8, 10 and 11 have been amended for which there is support in the specification, claims and drawings as originally filed. Claim 13 has been canceled without prejudice.

Reconsideration of the Examiner's decisions and reexamination of this application are respectfully requested.

A clean copy of the amended claims is included with this Amendment. A MARKED-UP VERSION SHOWING CHANGES MADE is included in the APPENDIX.

The §112 rejections

Claims 1, 3, 4, 10 and 11 have been rejected by the Examiner under 35 USC §112, second paragraph, as being indefinite. The Examiner alleges that the word "predetermined" as used in the claims is in error.

Applicants respectfully disagree with the Examiner. Applicants believe it is acceptable practice to use the term "predetermined" in the manner it is used in the claims. However, to

advance the prosecution of the claims, "predetermined" has been deleted from the claims.

With the amendments to the claims, the rejection of claims 1, 3, 4, 10 and 11 under 35 USC §112, second paragraph, is now moot.

The §103 rejections.

I. Claims 1, 4, 5 to 7, 8, 11, 12, 14 and 15 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk et al. U.S. Patent 5,340,437 (hereafter "Erk") in view of Barbee et al. U.S. Patent 5,445,705 (hereafter "Barbee").

The limitation of claim 13 has been added to claims 1 and 8. (Claim 13 has been canceled without prejudice.) Accordingly, both claims 1 and 8 are directed to improving the uniformity of etching of a film having a plurality of solder bumps.

It is noted that claim 13 was rejected under 35 USC §103(a) as being unpatentable over Erk in view of Barbee and further in view of Applicants' admitted prior art. Due to the inclusion of the subject matter of claim 13 into claims 1 and 8, it is assumed that claims 1 and 8 would similarly be rejected.

The rationale for the rejection of claim 13 was stated as follows.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Erk in view of Barbee by using a semiconductor wafer that comprises a plurality of solder bumps on a film, as shown in applicant's admitted prior art for the purpose of improving the method of placing more circuits on a chip.

It is respectfully submitted that the Examiner's rationale for the rejection of claim 13, and hence claims 1 and 8, is erroneous in at least three respects. The first is that Erk is directed to the etching of bare silicon wafers to remove any residual effects of sawing and lapping. It is to be assumed that as a result of the etching process in Erk, such residual effects would be removed. There is nothing in Erk to indicate that the teachings of Erk would be applicable to any other process other than the removal of such residual effects. And while Barbee teaches a film on a wafer and Applicants' admitted prior art teaches a plurality of solder bumps, there is no motivation ascertainable from any or all of the references that would lead to a combination of Erk, Barbee and Applicants' admitted prior art which would teach improving the uniformity of etching of a film having a plurality of solder bumps as claimed by Applicants.

Second, Applicants' claims 1 and 8 are directed to a "method of improving the uniformity of etching of a film having a plurality of solder bumps" [emphasis added]. Improving the uniformity of etching is an important limitation of Applicants' claims 1 and 8. While Erk appears to address thickness variations, both locally and across the entire wafer (col. 2, lines 22-29), this is not the same as uniformly etching a film across the entire wafer as taught by Applicants.

Third, the teaching of Applicants' invention is that the presence of the solder bumps complicates the etching of the metal films (specification page 3, lines 20-21). Thus, it cannot be assumed that the etching of a bare wafer as taught by Erk, even in view of a wafer having a film as taught by Barbee, would be applicable to the etching of a wafer with a film having a plurality of solder bumps. While Applicants' admitted prior art does disclose the etching of a film having a plurality of solder bumps on a wafer, that is all that it teaches. There is no teaching in Erk, Barbee and Applicants' admitted prior art to indicate that when the combination of references are viewed as a whole, they would be applicable to improving the uniformity of etching of a film having a plurality of solder bumps as claimed by Applicants.

In view of the preceding remarks, it is submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claims 1 and 8. Accordingly, claims 1 and 8 should be allowable.

Inasmuch as claims 4, 5 to 7, 11, 12, 14 and 15 depend from claims 1 and 8, and since claims 1 and 8 are believed to be allowable, then claims 4, 5 to 7, 11, 12, 14 and 15 should be allowable as well. No independent ground of patentability is asserted for claims 4, 5 to 7, 11, 12, 14 and 15 at this time.

II. Claims 2, 3, 9 and 10 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Barbee and further in view of Takeshi et al. (English Abstract of

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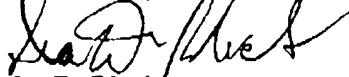
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Inasmuch as claims 2, 3, 9 and 10 depend from claims 1 and 8, and since claims 1 and 8 are believed to be allowable, then claims 2, 3, 9 and 10 should be allowable as well. No independent ground of patentability is asserted for claims 2, 3, 9 and 10 at this time.

Summary:

In view of all of the preceding remarks, it is submitted that claims 1 to 12 and 14 to 15 are in condition for allowance. If the Examiner finds this application deficient in any respect, the Examiner is invited to telephone the undersigned to resolve such deficiency.

Respectfully submitted,



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APPENDIX**MARKED-UP VERSION SHOWING CHANGES MADE**In the claims:

Cancel claim 13 without prejudice.

1. (Amended) A method of improving the uniformity of etching of a film having a plurality of solder bumps on an article, the method comprising the steps of:

immersing the article containing the film having a plurality of solder bumps into a tank of etchant;

rotating the article while in the etchant for [a predetermined] an amount of time so as to cause improved uniformity of etching of the film across the entire article compared to etching without rotating the article; and

removing the article from the tank of etchant.

3. (Amended) The method of claim 1 wherein the step of sequentially rotating comprises rotating the article [a predetermined] an amount but less than a complete rotation, etching the article [a predetermined] an amount of time, and repeating the steps of rotating and etching for [a predetermined] an amount of time.

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4. (Amended) The method of claim 1 wherein the step of rotating comprises continuously rotating the article [a predetermined] an amount of time.

8. (Amended) A method of improving the uniformity of etching of a film having a plurality of solder bumps on a semiconductor wafer, the method comprising the steps of:

immersing the semiconductor wafer containing the film having a plurality of solder bumps into a tank of etchant;

rotating the semiconductor wafer while in the etchant for [a predetermined] an amount of time;
and

removing the semiconductor wafer from the tank of etchant.

10. (Amended) The method of claim 8 wherein the step of sequentially rotating comprises rotating the semiconductor wafer [a predetermined] an amount but less than a complete rotation, etching the semiconductor wafer [a predetermined] an amount of time, and repeating the steps of rotating and etching for [a predetermined] an amount of time.

11. (Amended) The method of claim 8 wherein the step of rotating comprises continuously rotating the semiconductor wafer [a predetermined] an amount of time